Inter Office Memo

ATARI®

Home Computer Division

To: Don Lang

From: Bob Mizerek

Subject: 3600 ELECTRICAL DESIGN REVIEW Date: 9-22-83

A short Electrical Design Review Meeting was held on September 21, 1983, based on information from 3600 Schematic Rev. 5 (undated), and the following questions and concerns were raised:

A. Documentation Needed

1. Latest revised schematics.

2. System timing charts.

3. Functional description and block diagram of Maria chip.

B. Design Issues

1. Will provisions be made for jumpering out the power latch for manufacturing testing.

2. The power latch is CMOS and can be subjected to ESD.

3. The 6116 CMOS static RAMS are not buffered and can be subject to possible ESD. Raising the shield height around the cartridge part may help this problem.

4. Resistors should be added on the joystick lines to reduce ESD and RFI problems.

5. The joystick trigger lines have been connected to previously unused inputs on the 6532. This may cause a packaging problem (i.e. number of pins) on a potential 6502/6532 composite device.

6. The power adaptor connector on the base unit must not allow the connection of an Atari AC power adaptor (e.g. 800 power adaptor) because of safety hazards.

7. The two capacitors associated with the 14 MHz crystal should be returned directly to Vss on the Maria chip and not to any general ground location.

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cc: D. Stubben
T. Kennedy
A. De Schweinitz
C. Goy
W. Alexander
H. Kramer
G. Seymour
R. Coppock
B. Simmeth
T. Harbeck

General Computer

D. Schwinn
P. McCrea